

What is claimed is:

1 1. A method for receiving data from a plurality of
2 ports for processing by a plurality of processes,
3 comprising:

4 assigning one of the plurality of ports to one of the
5 plurality of processes;

6 determining that additional data is available from the
7 assigned port; and

8 awaiting notification by the one of the plurality of processes
9 that processing has been completed prior to re-assigning the port
0 to one of the plurality of processes.

1 2. The method of claim 1, further comprising:

2 determining if data is available from one of the plurality of
3 ports.

1 3. The method of claim 1, further comprising:

2 selecting one of the plurality of processes.

1 4. The method of claim 3, further comprising:

2 directing transfer of the data from the assigned port to the

3 one of the plurality of processes for processing.

1 5. The method of claim 3, wherein selecting comprises:
2 determining if any of the plurality of processes is available
3 to process the data; and
4 if it is determined that one of the plurality of processes is
5 available to process the data, choosing an available one of the
6 plurality of processes.

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6 6. The method of claim 1, further comprising:
recording the port-to-thread assignment on an assignment list.

7. The method of claim 6, further comprising:
removing the port-to-thread assignment from the
assignment list upon receiving notification that the processing
has been completed.

1 8. The method of claim 1, wherein the data comprises
2 packet data.

1 9. The method of claim 8, wherein the packet data
2 comprises a network packet.

1 10. The method of claim 9, wherein the packet data
2 comprises a predetermined portion of a network packet.

1 11. The method of claim 9, wherein the network packet
2 comprises an Ethernet packet.

1 C 12. The method of claim 1, wherein the one of the
2 plurality of ports comprises a 10/100 BaseT Ethernet port.

1 13. An article comprising a computer-readable medium
2 which stores computer-executable instructions for receiving data
3 from a plurality of ports for processing by a plurality of
4 processes, the instructions causing a computer to:
5 assign one of the plurality of ports to one of the
6 plurality of processes

7 determine that additional data is available from the one
8 of the plurality of ports; and

9 await notification by the process that processing has
10 been completed for the transferred data prior to re-assigning the
11 one of the plurality of ports to one of the plurality of
12 processes.

1 14. The article of claim 13, wherein the article further
2 comprises instructions causing a computer to:

3 determine if data is available from one of the plurality
4 if ports.

1 15. The article of claim 13, wherein the article further
2 comprises instructions causing a computer to:

3 select one of the plurality of processes.

4 16. The article of claim 15, wherein the instructions to
5 select one of the plurality of processes comprises instructions
6 causing a computer to:

7 determine if any of the plurality of processes is
8 available to process the data; and

9 choose an available one of the plurality of processes if
10 it is determined that one of the plurality of processes is
11 available to process the data.

1 17. The article of claim 13, wherein the article further
2 comprises instructions causing a computer to:

3 record the port-to-thread assignment on an assignment

4 list.

1 18. The article of claim 17, wherein the article further
2 comprises instructions causing a computer to:

3 remove the port-to-thread assignment from the assignment
4 list upon receiving notification that the processing has been
5 completed.

19. A processor comprising:

2 a microengine for executing threads, the threads
3 including a receive scheduler thread and receive processing
4 threads;

5 a bus interface for receiving data from a port, the bus
6 interface for indicating to the receive scheduler whether the
7 port has data available for processing by one of the receive
8 processing threads; and

9 the receive scheduler thread assigning the port to one of
10 the receive scheduling threads if the bus interface has indicated
11 that the port has available data and directing transfer of the
12 data to the assigned one of the receive processing threads for
13 processing, the receive scheduler thread inhibiting the
14 assignment of the port to one of the receive processing threads

15 for the processing of new data until the assigned one of the
16 receive processing threads has completed the processing of the
17 data.